Amendments to the Claims:

Please add new claims 79-92, as follows:

--79. A method of masking data coupled through a data output buffer responsive to a data mask signal applied to the output buffer, the output buffer having first and second stages connected in series with each other, the method comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and in response to a second clock edge of the clock signal for a second latency setting;

coupling first and second input terminals at which complimentary first and second data signals are applied, respectively, to respective first and second output terminals of the first stage when the data mask signal is inactive;

generating a control signal responsive to a predetermined portion of a clock signal after the data mask signal becomes active;

applying respective predetermined signals to the first and second output terminals of the first stage responsive to the control signal;

applying a data output signal to an output terminal of the second stage corresponding to the complimentary first and second data signals when the respective predetermined signals are not being applied to the first and second input terminals of the second stage; and

tri-stating the output terminal of the second stage when the respective predetermined signals are being applied to the first and second input terminals of the second stage.

80. The method of claim 79 wherein the respective predetermined signals applied to the first and second output terminals of the first stage are any signals that are not complimentary to each other.

81. The method of claim 80 wherein the predetermined signals correspond to logic "1".

82. The method of claim 79 wherein the coupling of the first and second input terminals to the respective first and second output terminals of the first stage is delayed in time so that the complimentary first and second data signals are stored in the first stage for a predetermined time.

83. A method of selectively masking complimentary read data signals responsive to a data mask signal, comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and in response to a second clock edge of the clock signal for a second latency setting;

generating coded read data signals corresponding to the complimentary read data signals in the absence of the data mask signal;

a predetermined period after receipt of the data mask signal, generating coded read data signals coded in a predetermined manner responsive to the data mask signal;

generating on a data output terminal an output signal having a value corresponding to the coded read data signals if the coded read data signals are not coded in the predetermined manner; and

placing the data output terminal at a high impedance if the coded read data signals are coded in the predetermined manner.

84. The method of claim 83 wherein the predetermined manner of coding is for the coded read data signals to have the same value.

85. A method of masking data coupled through a data output buffer responsive to a data mask signal applied to the output buffer, the output buffer having first and second stages connected in series with each other, the method comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and in response to a second clock edge of the clock signal for a second latency setting;

coupling first and second input terminals at which complimentary first and second data signals are applied, respectively, to respective first and second output terminals of the first stage to provide first and second read output signals, respectively, to the second stage when the data mask signal is inactive;

applying respective predetermined signals to the first and second output terminals of the first stage to provide the first and second read output signals, respectively, to the second stage when the data mask signal is active;

coupling an output terminal of the second stage to a first voltage node responsive to one of the data read output signals having a first predetermined logic level;

coupling the output terminal of the second stage to a second voltage node responsive to the other of the data read output signals having a second predetermined logic level; and

electrically isolating the output terminal of the second stage from the first and second voltage nodes responsive to both the data read output signals having other than the first or second predetermined logic levels.

86. The method of claim 85 wherein the respective predetermined signals applied to the first and second output terminals of the first stage are any signals that are not complimentary to each other.

87. The method of claim 86 wherein the predetermined signals correspond to logic "1".

88. The method of claim 85 wherein the coupling of the first and second input terminals to the respective first and second output terminals of the first stage is delayed in time so that the complimentary first and second data signals are stored in the first stage for a predetermined time.

89. A method of selectively masking complimentary read data signals responsive to a data mask signal, comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and in response to a second clock edge of the clock signal for a second latency setting;

generating first and second coded read data signals corresponding to the complimentary read data signals, respectively, in the absence of the data mask signal;

coding the first and second coded read data signals in a predetermined manner responsive to the data mask signal;

coupling a data output terminal to a first voltage node responsive to one of the coded read data signals having a first predetermined logic level;

coupling the data output terminal to a second voltage node responsive to the other of the coded read data signals having a second predetermined logic level; and

electrically isolating the data output terminal from the first and second voltage nodes if the coded read data signals are coded in the predetermined manner.

90. The method of claim 89 wherein the predetermined manner of coding is for the coded read data signals to have the same value.

91. A method of selectively masking complimentary read data signals responsive to a data mask signal, comprising:

registering a signal representing the data mask signal in response to a first clock edge of a clock signal for a first latency setting and in response to a second clock edge of the clock signal for a second latency setting;

generating coded read data signals corresponding to the complimentary read data signals in the absence of the data mask signal;

generating coded read data signals coded in a predetermined manner responsive to the data mask signal;

coupling a data output terminal to a first voltage node responsive to one of the coded read data signals having a first predetermined logic level;

coupling the data output terminal to a second voltage node responsive to the other of the coded read data signals having a second predetermined logic level; and